
4-Mbit SPI Serial Flash

Features

- Single Voltage Read and Write Operations:
 - 2.7V-3.6V
- Serial Interface Architecture:
 - SPI Compatible: Mode 0 and Mode 3
- High-Speed Clock Frequency:
 - Up to 50 MHz
- Superior Reliability:
 - Endurance: 100,000 Cycles (typical)
 - Greater than 100 years Data Retention
- Low-Power Consumption:
 - Active Read Current: 10 mA (typical)
 - Standby Current: 5 μ A (typical)
- Flexible Erase Capability:
 - Uniform 4-Kbyte sectors
 - Uniform 32-Kbyte overlay blocks
 - Uniform 64-Kbyte overlay blocks
- Fast Erase and Byte Program:
 - Chip Erase Time: 35 ms (typical)
 - Sector/Block Erase Time: 18 ms (typical)
 - Byte Program Time: 7 μ s (typical)
- Auto Address Increment (AAI) Programming:
 - Decrease total chip programming time over Byte Program operations
- End of Write Detection:
 - Software polling the BUSY bit in STATUS Register
 - Busy Status readout on SO pin in AAI Mode
- Hold Pin (HOLD#):
 - Suspends a serial sequence to the memory without deselecting the device
- Write Protection (WP#):
 - Enables/Disables the Lock-Down function of the STATUS register
- Software Write Protection:
 - Write protection through Block Protection bits in STATUS register
- Temperature Range:
 - Commercial: 0°C to +70°C
 - Industrial: -40°C to +85°C
- All devices are RoHS compliant

Packages

- 8-Lead SOIC (208 mils), 8-Lead SOIC (150 mils) and 8-Contact WSON (6 mm x 5 mm)

Description

The 25 series Serial Flash family features a four-wire, SPI-compatible interface that allows for a low pin-count package which occupies less board space and ultimately lowers total system costs. The SST25VF040B devices are enhanced with improved operating frequency and even lower power consumption. SST25VF040B SPI serial Flash memories are manufactured with proprietary, high-performance CMOS SuperFlash[®] technology. The split-gate cell design and thick-oxide tunneling injector attain better reliability and manufacturability compared with alternate approaches.

SST25VF040B devices significantly improve performance and reliability, while lowering power consumption. The devices write (Program or Erase) with a single power supply of 2.7V-3.6V for SST25VF040B. The total energy consumed is a function of the applied voltage, current, and time of application. Since for any given voltage range, the SuperFlash technology uses less current to program and has a shorter erase time, the total energy consumed during any erase or program operation is less than alternative Flash memory technologies.

See [Figure 2-1](#) for pin assignments.

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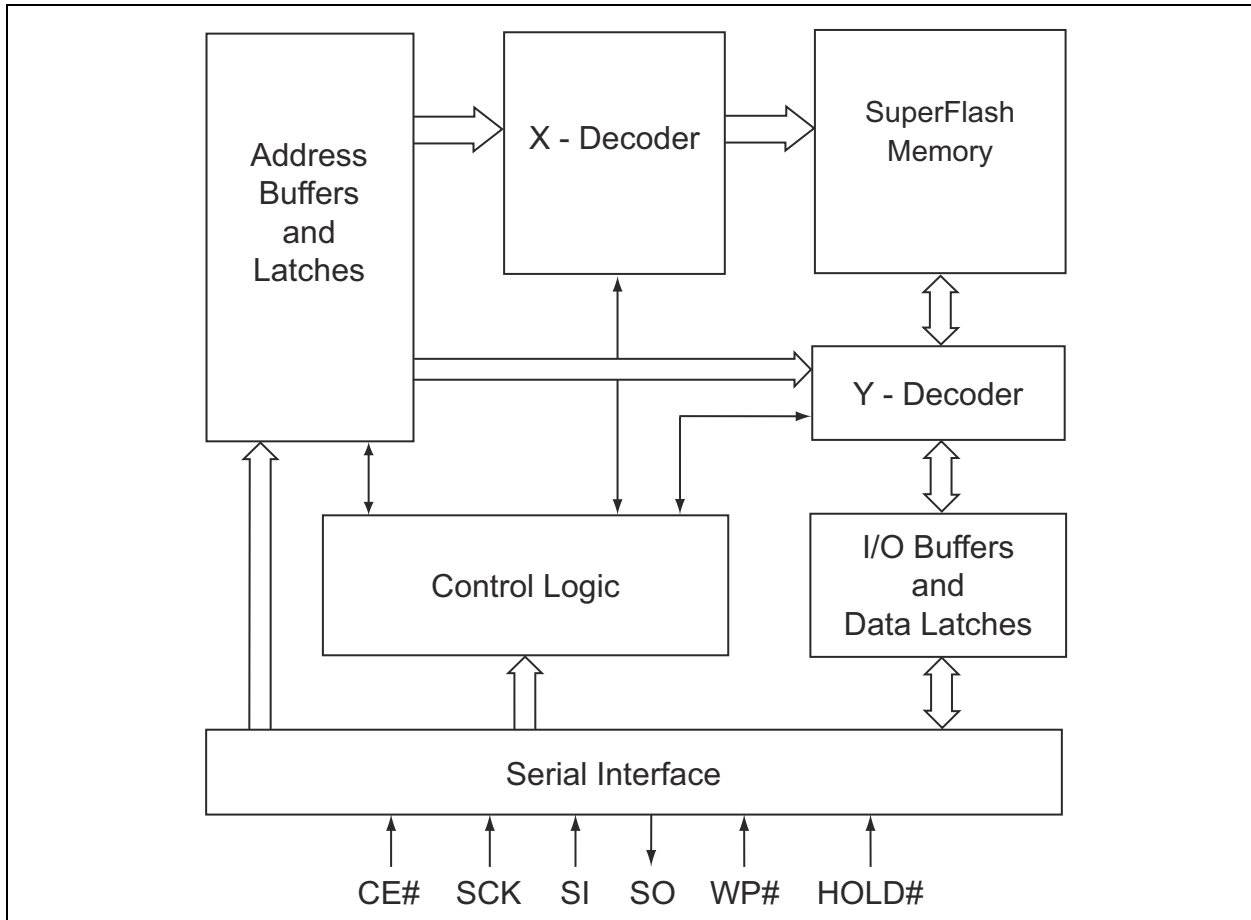
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1.0 BLOCK DIAGRAM

FIGURE 1-1: FUNCTIONAL BLOCK DIAGRAM



2.0 PIN DESCRIPTION

FIGURE 2-1: PIN ASSIGNMENTS

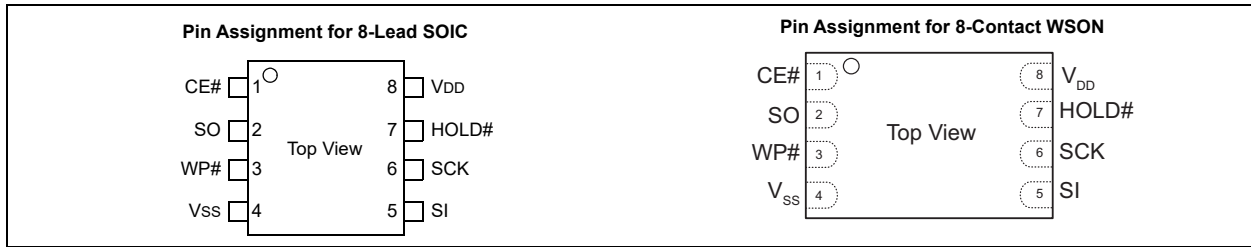


TABLE 2-1: PIN DESCRIPTION

Symbol	Pin Name	Functions
CE#	Chip Enable	The device is enabled by a high to low transition on CE#. CE# must remain low for the duration of any command sequence.
SO	Serial Data Output	To transfer data serially out of the device. Data is shifted out on the falling edge of the serial clock. Outputs Flash busy status during AAI Programming when reconfigured as RY/BY# pin. See Section 5.5 “End of Write Detection” for details.
WP#	Write-Protect	The Write-Protect (WP#) pin is used to enable/disable BPL bit in the STATUS register.
Vss	Ground	
VDD	Power Supply	To provide power supply voltage:2.7V-3.6V for SST25VF040B.
HOLD#	Hold	To temporarily stop serial communication with SPI Flash memory without resetting the device.
SCK	Serial Clock	To provide the timing of the serial interface. Commands, addresses, or input data are latched on the rising edge of the clock input, while output data is shifted out on the falling edge of the clock input.
SI	Serial Data Input	To transfer commands, addresses, or data serially into the device. Inputs are latched on the rising edge of the serial clock.

3.0 MEMORY ORGANIZATION

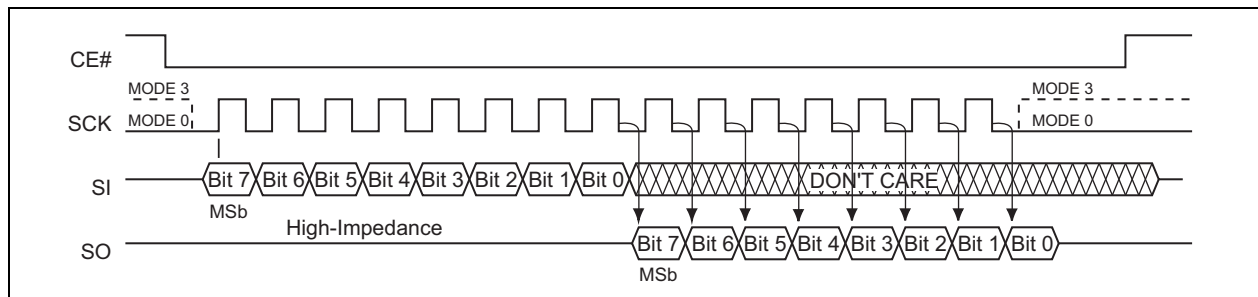
The SST25VF040B SuperFlash memory array is organized in uniform 4-Kbyte erasable sectors with 32-Kbyte overlay blocks and 64-Kbyte overlay erasable blocks.

4.0 DEVICE OPERATION

The SST25VF040B is accessed through the SPI (Serial Peripheral Interface) bus compatible protocol. The SPI bus consist of four control lines; Chip Enable (CE#) is used to select the device, and data is accessed through the Serial Data Input (SI), Serial Data Output (SO), and Serial Clock (SCK).

The SST25VF040B supports both Mode 0 (0,0) and Mode 3 (1,1) of SPI bus operations. The difference between the two modes, as shown in [Figure 4-1](#), is the state of the SCK signal when the bus master is in Stand-by mode and no data is being transferred. The SCK signal is low for Mode 0 and SCK signal is high for Mode 3. For both modes, the Serial Data In (SI) is sampled at the rising edge of the SCK clock signal and the Serial Data Output (SO) is driven after the falling edge of the SCK clock signal.

FIGURE 4-1: SPI PROTOCOL



4.1 Hold Operation

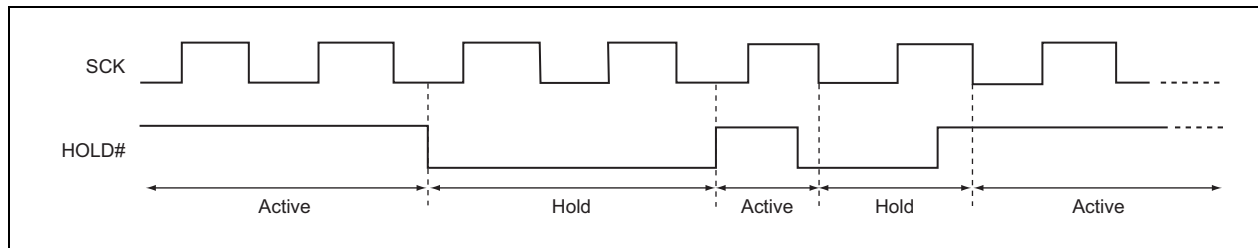
The HOLD# pin is used to pause a serial sequence underway with the SPI Flash memory without resetting the clocking sequence. To activate the HOLD# mode, CE# must be in active-low state. The HOLD# mode begins when the SCK active-low state coincides with the falling edge of the HOLD# signal. The HOLD mode ends when the HOLD# signal's rising edge coincides with the SCK active-low state.

Once the device enters Hold mode, SO will be in high-impedance state while SI and SCK can be V_{IL} or V_{IH}.

If the falling edge of the HOLD# signal does not coincide with the SCK active-low state, then the device enters Hold mode when the SCK next reaches the active-low state. Similarly, if the rising edge of the HOLD# signal does not coincide with the SCK active-low state, then the device exits in Hold mode when the SCK next reaches the active-low state. See [Figure 4-2](#) for Hold Condition waveform.

If CE# is driven active-high during a Hold condition, it resets the internal logic of the device. As long as HOLD# signal is low, the memory remains in the Hold condition. To resume communication with the device, HOLD# must be driven active-high, and CE# must be driven active-low. See [Figure 8-3](#) for Hold timing.

FIGURE 4-2: HOLD CONDITION WAVEFORM



4.2 Write Protection

SST25VF040B provides software write protection. The Write-Protect pin (WP#) enables or disables the lock-down function of the STATUS register. The Block Protection bits (BP3, BP2, BP1, BP0, and BPL) in the STATUS register provide Write protection to the memory array and the STATUS register. See [Table 4-3](#) for the Block Protection description.

4.2.1 WRITE PROTECTION PIN (WP#)

The Write-Protect (WP#) pin enables the lock-down function of the BPL bit (bit 7) in the STATUS register. When WP# is driven low, the execution of the Write STATUS Register ($WRSR$) instruction is determined by the value of the BPL bit (see [Table 4-1](#)). When WP# is high, the lock-down function of the BPL bit is disabled.

TABLE 4-1: CONDITIONS TO EXECUTE WRITE STATUS REGISTER ($WRSR$) INSTRUCTIONS

WP#	BPL	Execute $WRSR$ Instructions
L	1	Not Allowed
L	0	Allowed
H	X	Allowed

4.3 STATUS Register

The software STATUS register provides status on whether the Flash memory array is available for any read or write operation, whether the device is write enabled and the state of the Memory Write-protected.

During an internal erase or program operation, the STATUS register may be read only to determine the completion of an operation in progress. [Table 4-2](#) describes the function of each bit in the software STATUS register.

TABLE 4-2: SOFTWARE STATUS REGISTER

Bit	Name	Function	Default at Power-Up	Read/Write
0	BUSY	1 = Internal Write operation is in progress 0 = No internal Write operation is in progress	0	R
1	WEL	1 = Device is memory Write enabled 0 = Device is not memory Write enabled	0	R
2	BP0	Indicate current level of block write protection (see Table 4-3)	1	R/W
3	BP1	Indicate current level of block write protection (see Table 4-3)	1	R/W
4	BP2	Indicate current level of block write protection (see Table 4-3)	1	R/W
5	BP3	Indicate current level of block write protection (see Table 4-3)	0	R/W
6	AAI	Auto Address Increment Programming status 1 = AAI programming mode 0 = Byte Program mode	0	R
7	BPL	1 = BP3, BP2, BP1, BP0 are read-only bits 0 = BP3, BP2, BP1, BP0 are read/writable	0	R/W

4.3.1 BUSY

The BUSY bit determines whether there is an internal Erase or Program operation in progress. A '1' for the BUSY bit indicates the device is busy with an operation in progress. A '0' indicates the device is ready for the next valid operation.

The Write Enable Latch bit is automatically reset under the following conditions:

- Power-up
- Write Disable ($WRDI$) instruction completion
- Byte Program instruction completion
- Auto Address Increment (AAI) programming is completed or reached its highest unprotected memory address
- Sector Erase instruction completion
- Block Erase instruction completion
- Chip Erase instruction completion
- Write STATUS register instructions

4.3.2 WRITE ENABLE LATCH (WEL)

The Write Enable Latch bit indicates the status of the internal memory Write Enable Latch. If the Write Enable Latch bit is set to '1', it indicates the device is Write enabled. If the bit is set to '0' (reset), it indicates the device is not write enabled and does not accept any memory write (program/erase) commands.

4.3.3 AUTO ADDRESS INCREMENT (AAI)

The Auto Address Increment Programming Status bit provides status on whether the device is in AAI programming mode or Byte-Program mode. The default at power up is Byte-Program mode.

4.3.4 BLOCK PROTECTION (BP3, BP2, BP1, BP0)

The Block Protection (BP3, BP2, BP1, BP0) bits define the size of the memory area, as defined in Table 4-3, to be software protected against any memory write (program or erase) operation. The Write STATUS Register (WRSR) instruction is used to program the BP3, BP2, BP1 and BP0 bits as long as WP# is high or the Block Protect Lock (BPL) bit is '0'. Chip Erase can only be executed if Block Protection bits are all '0'. After power-up, BP3, BP2, BP1 and BP0 are set to '1'.

4.3.5 BLOCK PROTECTION LOCK-DOWN (BPL)

WP# pin driven low (V_{IL}), enables the Block Protection Lock Down (BPL) bit. When BPL is set to '1', it prevents any further alteration of the BPL, BP3, BP2, BP1, and BP0 bits. When the WP# pin is driven high (V_{IH}), the BPL bit has no effect and its value is "don't care". After power-up, the BPL bit is reset to '0'.

TABLE 4-3: SOFTWARE STATUS REGISTER BLOCK PROTECTION FOR SST25VF040B⁽¹⁾

Protection Level	STATUS Register Bit				Protected Memory Address
	BP3	BP2 ⁽²⁾	BP1 ⁽²⁾	BP0 ⁽²⁾	4 Mbits
None	X	0	0	0	None
Upper 1/16	X	0	0	1	70000H-7FFFFH
Upper 1/8	X	0	1	0	60000H-7FFFFH
Upper 1/4	X	0	1	1	40000H-7FFFFH
Upper 1/2	X	1	0	0	00000H-7FFFFH
All Blocks	X	1	0	1	00000H-7FFFFH
All Blocks	X	1	1	0	00000H-7FFFFH
All Blocks	X	1	1	1	00000H-7FFFFH

Note 1: X = "Don't care" (RESERVED) default is '0'.

2: Default at power-up for BP2, BP1, and BP0 is '111'. (All Blocks Protected)

5.0 INSTRUCTIONS

Instructions are used to read, write (Erase and Program), and configure the SST25VF040B. The instruction bus cycles are 8 bits each for commands (Op Code), data, and addresses. Prior to executing any Byte Program, Auto Address Increment (AAI) programming, Sector Erase, Block Erase, Write STATUS Register, or Chip Erase instructions, the Write Enable (WREN) instruction must be executed first. The complete list of instructions is provided in [Table 5-1](#). All instructions are synchronized off a high-to-low transition of CE#. Inputs will be accepted on the rising edge of SCK starting with the most significant bit. CE# must be driven low before an instruction is entered and must be driven high after the last bit of the instruction has been shifted in (except for Read, Read ID, and Read STATUS Register instructions). Any low-to-high transition on CE#, before receiving the last bit of an instruction bus cycle, will terminate the instruction in progress and return the device to standby mode. Instruction commands (Op Code), addresses, and data are all input from the most significant bit (MSb) first.

TABLE 5-1: DEVICE OPERATION INSTRUCTION

Instruction	Description	Op Code Cycle ⁽¹⁾	Address Cycle(s) ⁽²⁾	Dummy Cycle(s)	Data Cycle(s)
Read	Read Memory	0000 0011b (03H)	3	0	1 to ∞
High-Speed Read	Read Memory at higher speed	0000 1011b (0BH)	3	1	1 to ∞
4-Kbyte Sector Erase ⁽³⁾	Erase 4-Kbyte of memory array	0010 0000b (20H)	3	0	0
32-Kbyte Block Erase ⁽⁴⁾	Erase 32-Kbyte block of memory array	0101 0010b (52H)	3	0	0
64-Kbyte Block Erase ⁽⁵⁾	Erase 64-Kbyte block of memory array	1101 1000b (D8H)	3	0	0
Chip-Erase	Erase Full Memory Array	0110 0000b (60H) or 1100 0111b (C7H)	0	0	0
Byte Program	To Program One Data Byte	0000 0010b (02H)	3	0	1
AAI Word Program ⁽⁶⁾	Auto Address Increment Programming	1010 1101b (ADH)	3	0	2 to ∞
RDSR ⁽⁷⁾	Read STATUS Register	0000 0101b (05H)	0	0	1 to ∞
EWSR	Enable Write STATUS Register	0101b 0000b (50H)	0	0	0
WRSR	Write STATUS Register	0000 0001b (01H)	0	0	1
WREN	Write Enable	0000 0110b (06H)	0	0	0
WRDI	Write Disable	0000 0100b (04H)	0	0	0
RDID ⁽⁸⁾	Read ID	1001 0000b (90H) or 1010 1011b (ABH)	3	0	1 to ∞
JEDEC-ID	JEDEC ID read	1001 1111b (9FH)	0	0	3 to ∞
EBSY	Enable SO to output RY/BY# status during AAI programming	0111 0000b (70H)	0	0	0
DBSY	Disable SO as RY/BY# status during AAI programming	1000 0000b (80H)	0	0	0

TABLE 5-1: DEVICE OPERATION INSTRUCTION

Instruction	Description	Op Code Cycle ⁽¹⁾	Address Cycle(s) ⁽²⁾	Dummy Cycle(s)	Data Cycle(s)
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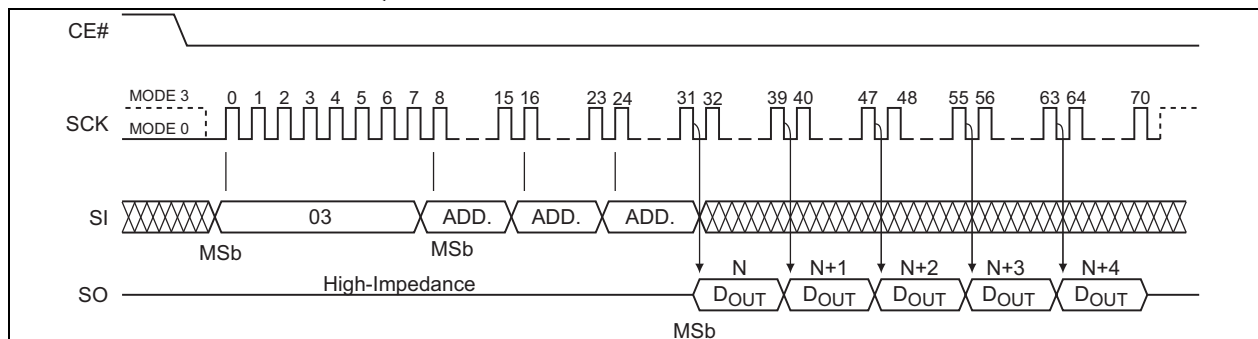
- Note 1:** One bus cycle is eight clock periods.
- 2:** Address bits above the most significant bit of each density can be VIL or VIH.
- 3:** 4-Kbyte Sector Erase addresses: use AMS-A12, remaining addresses are “don’t care” but must be set either at VIL or VIH.
- 4:** 32-Kbyte Block Erase addresses: use AMS-A15, remaining addresses are “don’t care” but must be set either at VIL or VIH.
- 5:** 64-Kbyte Block Erase addresses: use AMS-A16, remaining addresses are “don’t care” but must be set either at VIL or VIH.
- 6:** To continue programming to the next sequential address location, enter the 8-bit command, ADH, followed by 2 bytes of data to be programmed. Data Byte 0 will be programmed into the initial address [A23-A1] with A0 = 0, Data Byte 1 will be programmed into the initial address [A23-A1] with A0 = 1.
- 7:** The Read STATUS Register is continuous with ongoing clock cycles until terminated by a low-to-high transition on CE#.
- 8:** Manufacturer’s ID is read with A0 = 0, and Device ID is read with A0 = 1. All other address bits are 00H. The Manufacturer’s ID and device ID output stream is continuous until terminated by a low-to-high transition on CE#.

5.1 Read (25 MHz)

The Read instruction, 03H, supports up to 25 MHz Read. The device outputs the data starting from the specified address location. The data output stream is continuous through all addresses until terminated by a low-to-high transition on CE#. The internal address pointer will automatically increment until the highest memory address is reached. Once the highest memory address is reached, the address pointer will automatically increment to the beginning (wrap-around) of the address space. Once the data from address location 1FFFFFFH has been read, the next output will be from address location 00000H.

The Read instruction is initiated by executing an 8-bit command, 03H, followed by address bits [A23-A0]. CE# must remain active-low for the duration of the Read cycle. See Figure 5-1 for the Read sequence.

FIGURE 5-1: READ SEQUENCE



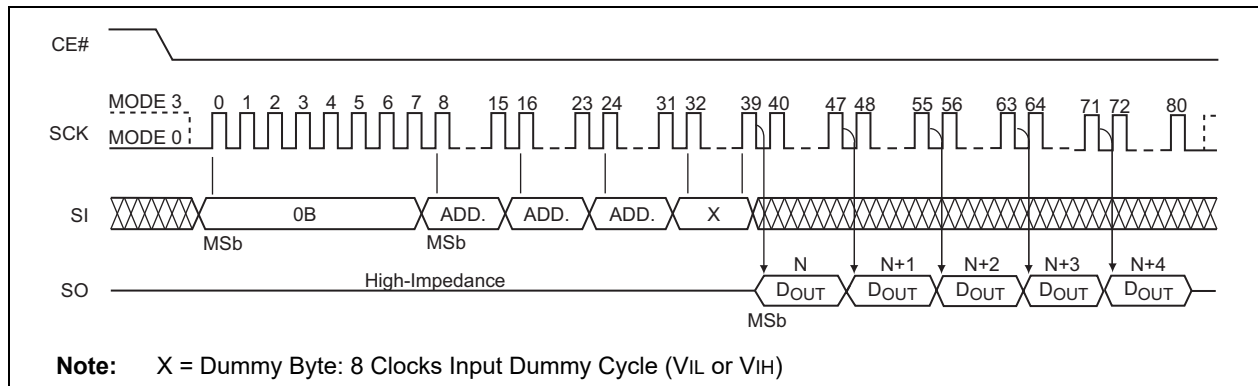
5.2 High-Speed Read (50 MHz)

The High-Speed Read instruction, supporting up to 50 MHz Read, is initiated by executing an 8-bit command, 0BH, followed by address bits [A23-A0] and a dummy byte. CE# must remain active-low for the duration of the High-Speed Read cycle. See Figure 5-2 for the High-Speed Read sequence.

Following a dummy cycle, the High-Speed Read instruction outputs the data starting from the specified address location. The data output stream is continuous through all addresses until terminated by a low-to-high transition on CE#.

The internal address pointer will automatically increment until the highest memory address is reached. Once the highest memory address is reached, the address pointer will automatically increment to the beginning (wrap-around) of the address space. Once the data from address location 7FFFFH has been read, the next output will be from address location 00000H.

FIGURE 5-2: HIGH-SPEED READ SEQUENCE



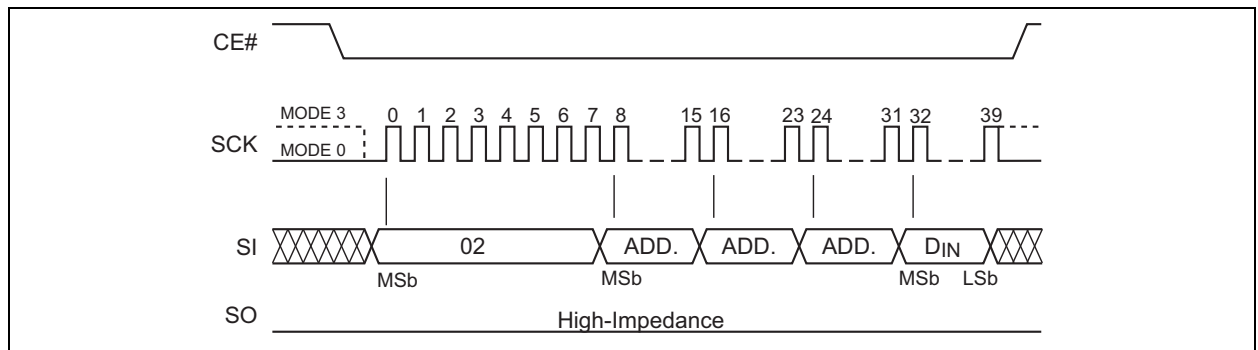
5.3 Byte Program

The Byte Program instruction programs the bits in the selected byte to the desired data. The selected byte must be in the erased state (FFH) when initiating a Program operation. A Byte Program instruction applied to a protected memory area will be ignored.

Prior to any write operation, the Write Enable (WREN) instruction must be executed. CE# must remain active-low for the duration of the Byte Program instruction.

The Byte Program instruction is initiated by executing an 8-bit command, 02H, followed by address bits [A23-A0]. Following the address, the data is input in order from MSb (bit 7) to LSb (bit 0). CE# must be driven high before the instruction is executed. The user may poll the BUSY bit in the software STATUS register or wait TBP for the completion of the internal self-timed Byte Program operation. See Figure 5-3 for the Byte Program sequence.

FIGURE 5-3: BYTE PROGRAM SEQUENCE



5.4 Auto Address Increment (AAI) Word Program

The AAI program instruction allows multiple bytes of data to be programmed without re-issuing the next sequential address location. This feature decreases total programming time when multiple bytes or entire memory array is to be programmed. An AAI Word program instruction pointing to a protected memory area will be ignored. The selected address range must be in the erased state (FFH) when initiating an AAI Word Program operation. While within AAI Word programming sequence, only the following instructions are valid: for software end of write detection—AAI Word (ADH), `WRDI` (04H), and `RDSR` (05H); for hardware end of write detection—AAI Word (ADH) and `WRDI` (04H). There are three options to determine the completion of each AAI Word program cycle: hardware detection by reading the Serial Output, software detection by polling the BUSY bit in the software STATUS register, or wait TBP. Refer to **Section 5.5 “End of Write Detection”** for details.

Prior to any write operation, the Write Enable (WREN) instruction must be executed. Initiate the AAI Word Program instruction by executing an 8-bit command, ADH, followed by address bits [A23-A0]. Following the addresses, two bytes of data are input sequentially, each one from MSb (Bit 7) to LSb (Bit 0). The first byte of data (D0) is programmed into the initial address [A23-A1] with A0 = 0, the second byte of Data (D1) is programmed into the initial address [A23-A1] with A0 = 1. CE# must be driven high before executing the AAI Word Program instruction. Check the Busy status before entering the next valid command. Once the device indicates it is no longer busy, data for the next two sequential addresses may be programmed, followed by the next two, and so on.

When programming the last desired word, or the highest unprotected memory address, check the busy status using either the hardware or software (`RDSR` instruction) method to check for program completion. Once programming is complete, use the applicable method to terminate AAI. If the device is in Software End of Write Detection mode, execute the Write Disable (`WRDI`) instruction, 04H. If the device is in AAI Hardware End of Write Detection mode, execute the Write Disable (`WRDI`) instruction, 04H, followed by the 8-bit DBSY command, 80H. There is no wrap mode during AAI programming once the highest unprotected memory address is reached. See [Figure 5-6](#) and [Figure 5-7](#) for the AAI Word programming sequence.

5.5 End of Write Detection

There are three methods to determine completion of a program cycle during AAI Word programming: hardware detection by reading the Serial Output, software detection by polling the BUSY bit in the software STATUS register, or wait TBP. The Hardware End of Write detection method is described in the section below.

5.6 Hardware End of Write Detection

The Hardware End of Write detection method eliminates the overhead of polling the BUSY bit in the software STATUS register during an AAI Word program operation. The 8-bit command, 70H, configures the Serial Output (SO) pin to indicate Flash Busy status during AAI Word programming (see [Figure 5-4](#)).

The 8-bit command, 70H, must be executed prior to initiating an AAI Word Program instruction. Once an internal programming operation begins, asserting CE# will immediately drive the status of the internal Flash status on the SO pin. A '0' indicates the device is busy and a '1' indicates the device is ready for the next instruction. De-asserting CE# will return the SO pin to tri-state. While in AAI and Hardware End of Write detection mode, the only valid instructions are AAI Word (ADH) and `WRDI` (04H).

To exit AAI Hardware End of Write detection, first execute `WRDI` instruction, 04H, to reset the Write Enable Latch bit (`WEL` = 0) and AAI bit. Then execute the 8-bit DBSY command, 80H, to disable RY/BY# status during the AAI command. See [Figure 5-5](#) and [Figure 5-6](#).

FIGURE 5-4: ENABLE SO AS HARDWARE RY/BY# DURING AAI PROGRAMMING

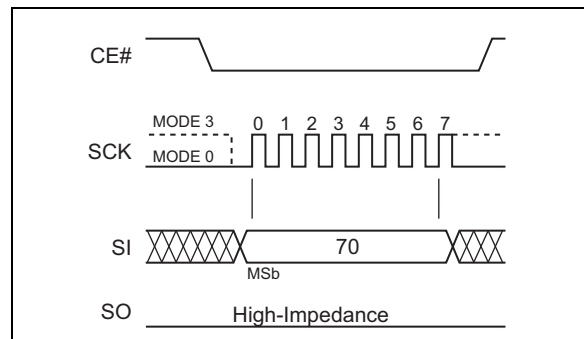


FIGURE 5-5: DISABLE SO AS HARDWARE RY/BY# DURING AAI PROGRAMMING

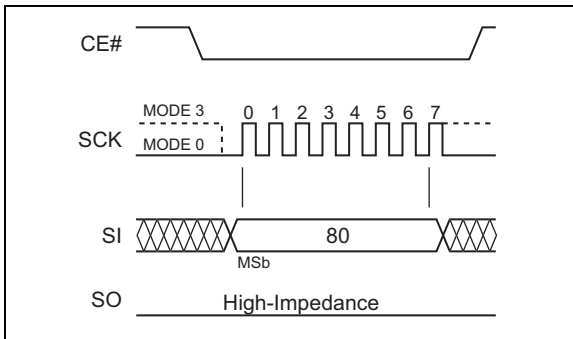
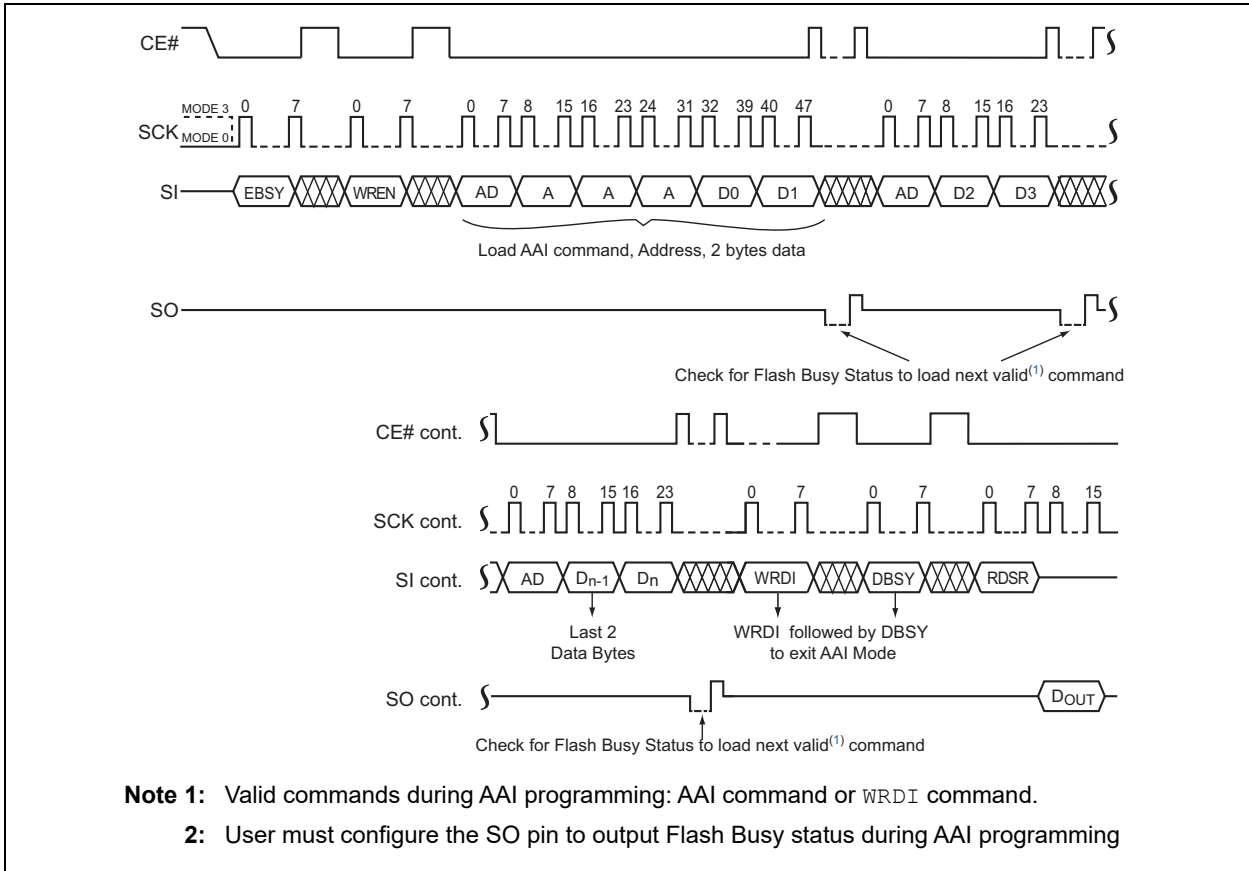
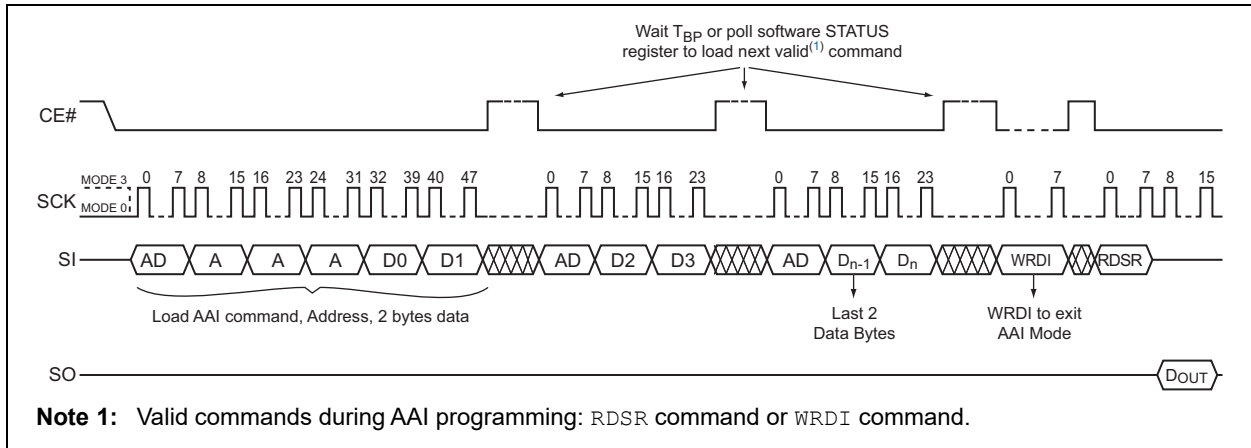


FIGURE 5-6: AUTO ADDRESS INCREMENT (AAI) WORD PROGRAM SEQUENCE WITH HARDWARE END OF WRITE DETECTION



- Note 1:** Valid commands during AAI programming: AAI command or `WRDI` command.
2: User must configure the SO pin to output Flash Busy status during AAI programming

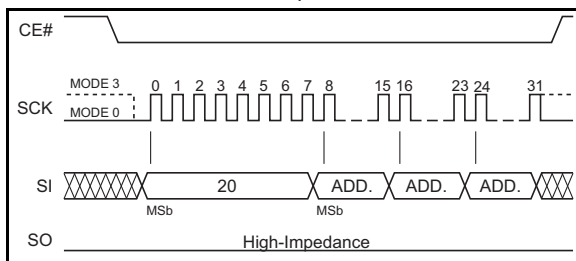
FIGURE 5-7: AUTO ADDRESS INCREMENT (AAI) WORD PROGRAM SEQUENCE WITH SOFTWARE END OF WRITE DETECTION



5.7 4-KByte Sector Erase

The Sector Erase instruction clears all bits in the selected 4-Kbyte sector to FFH. A Sector Erase instruction applied to a protected memory area will be ignored. Prior to any Write operation, the Write Enable (\overline{WREN}) instruction must be executed. CE# must remain active-low for the duration of any command sequence. The Sector Erase instruction is initiated by executing an 8-bit command, 20H, followed by address bits [A23-A0]. Address bits [AMS-A12] (AMS = Most Significant address) are used to determine the sector address (SAX), remaining address bits can be VIL or VIH. CE# must be driven high before the instruction is executed. The user may poll the BUSY bit in the software STATUS register or wait TSE for the completion of the internal self-timed Sector Erase cycle. See Figure 5-8 for the Sector Erase sequence.

FIGURE 5-8: SECTOR ERASE SEQUENCE



5.8 32-Kbyte and 64-Kbyte Block Erase

The 32-Kbyte Block Erase instruction clears all bits in the selected 32 Kbyte block to FFH. A Block Erase instruction applied to a protected memory area will be ignored. The 64-Kbyte Block-Erase instruction clears all bits in the selected 64 Kbyte block to FFH. A Block Erase instruction applied to a protected memory area will be ignored.

Prior to any Write operation, the Write Enable (\overline{WREN}) instruction must be executed. CE# must remain active-low for the duration of any command sequence. The 32-Kbyte Block Erase instruction is initiated by executing an 8-bit command, 52H, followed by address bits [A23-A0]. Address bits [AMS-A15] (AMS = Most Significant Address) are used to determine block address (BAX), remaining address bits can be VIL or VIH. CE# must be driven high before the instruction is executed. The 64-Kbyte Block Erase instruction is initiated by executing an 8-bit command D8H, followed by address bits [A23-A0]. Address bits [AMS-A15] are used to determine block address (BAX) while remaining address bits can be VIL or VIH. CE# must be driven high before the instruction is executed. The user may poll the BUSY bit in the software STATUS register or wait TBE for the completion of the internal self-timed 32-Kbyte Block Erase or 64-Kbyte Block Erase cycles. See Figure 5-9 and Figure 5-10 for the 32-Kbyte Block Erase and 64-Kbyte Block Erase sequences.

FIGURE 5-9: 32-KBYTE BLOCK ERASE SEQUENCE

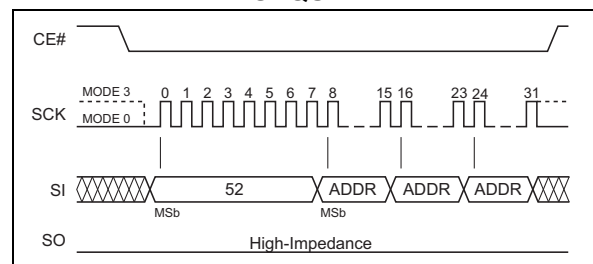
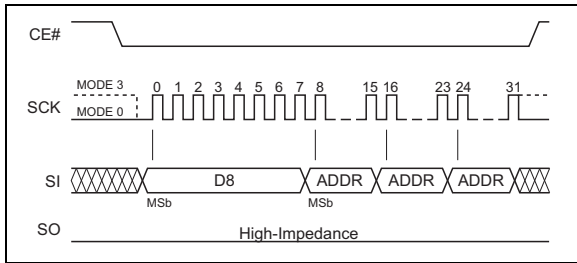


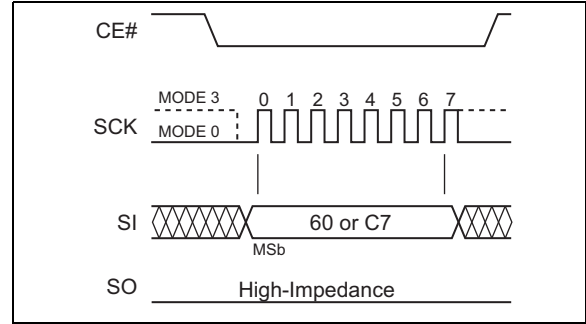
FIGURE 5-10: 64-KBYTE BLOCK ERASE SEQUENCE



5.9 Chip Erase

The Chip Erase instruction clears all bits in the device to FFH. A Chip Erase instruction will be ignored if any of the memory area is protected. Prior to any Write operation, the Write Enable (WREN) instruction must be executed. CE# must remain active-low for the duration of the Chip Erase instruction sequence. The Chip Erase instruction is initiated by executing an 8-bit command, 60H or C7H. CE# must be driven high before the instruction is executed. The user may poll the BUSY bit in the software STATUS register or wait TCE for the completion of the internal self-timed Chip Erase cycle. See Figure 5-11 for the Chip Erase sequence.

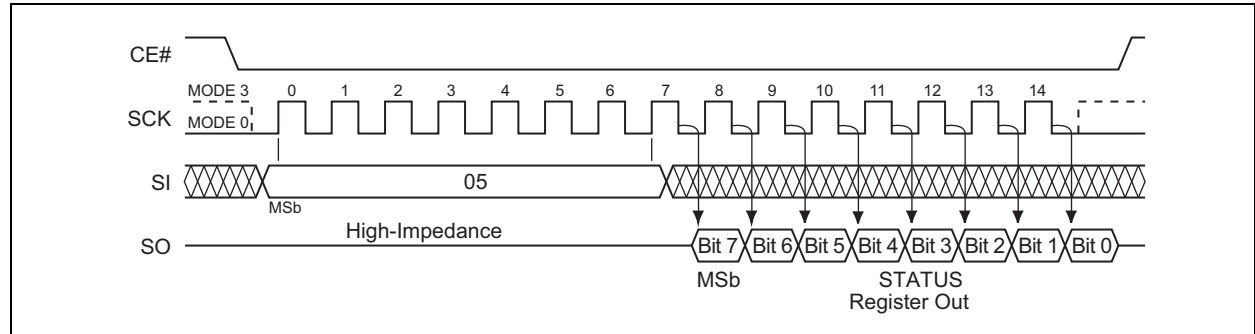
FIGURE 5-11: CHIP ERASE SEQUENCE



5.10 Read STATUS Register (RDSR)

The Read STATUS Register (RDSR) instruction allows reading of the STATUS register. The STATUS register may be read at any time even during a write (program/erase) operation. When a write operation is in progress, the BUSY bit may be checked before sending any new commands to assure that the new commands are properly received by the device. CE# must be driven low before the RDSR instruction is entered and remain low until the status data is read. Read STATUS register is continuous with ongoing clock cycles until it is terminated by a low-to-high transition of the CE#. See Figure 5-12 for the RDSR instruction sequence.

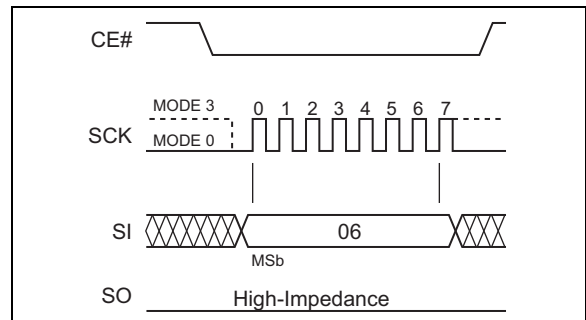
FIGURE 5-12: READ STATUS REGISTER (RDSR) SEQUENCE



5.11 Write Enable (WREN) Sequence

The Write Enable (WREN) instruction sets the Write Enable Latch bit in the STATUS register to '1' allowing write operations to occur. The WREN instruction must be executed prior to any write (program/erase) operation. The WREN instruction may also be used to allow execution of the Write STATUS Register (WRSR) instruction; however, the Write Enable Latch bit in the STATUS register will be cleared upon the rising edge CE# of the WRSR instruction. CE# must be driven high before the WREN instruction is executed.

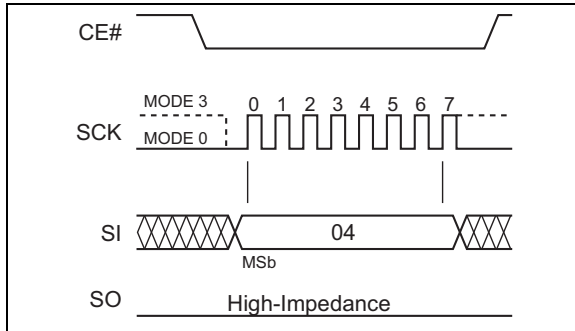
FIGURE 5-13: WRITE ENABLE (WREN) SEQUENCE



5.12 Write Disable (WRDI)

The Write Disable (WRDI) instruction resets the Write Enable-Latch bit and AAI bit to '0' disabling any new Write operations from occurring. The WRDI instruction will not terminate any programming operation in progress. Any program operation in progress may continue up to TBP after executing the WRDI instruction. CE# must be driven high before the WRDI instruction is executed.

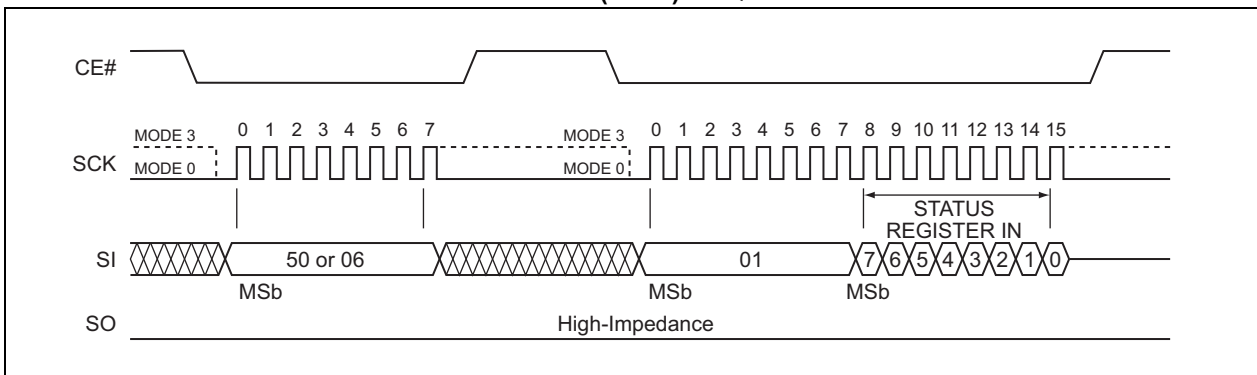
FIGURE 5-14: WRITE DISABLE (WRDI) SEQUENCE



5.13 Enable Write STATUS Register (EWSR)

The Enable Write STATUS Register (EWSR) instruction arms the Write STATUS Register (WRSR) instruction and opens the STATUS register for alteration. The Write STATUS Register instruction must be executed immediately after the execution of the Enable Write STATUS Register instruction.

FIGURE 5-15: ENABLE WRITE STATUS REGISTER (EWSR) OR WRITE ENABLE (WREN) AND WRITE STATUS REGISTER (WRSR) SEQUENCE



This two-step instruction sequence of the EWSR instruction followed by the WRSR instruction works like SDP (software data protection) command structure which prevents any accidental alteration of the STATUS register values. CE# must be driven low before the EWSR instruction is entered and must be driven high before the EWSR instruction is executed.

5.14 Write STATUS Register (WRSR)

The Write STATUS Register instruction writes new values to the BP3, BP2, BP1, BP0, and BPL bits of the STATUS register. CE# must be driven low before the command sequence of the WRSR instruction is entered and driven high before the WRSR instruction is executed. See Figure 5-15 for EWSR or WREN and WRSR instruction sequences.

Executing the Write STATUS Register instruction will be ignored when WP# is low and BPL bit is set to '1'. When the WP# is low, the BPL bit can only be set from '0' to '1' to lock-down the STATUS register, but cannot be reset from '1' to '0'. When WP# is high, the lock-down function of the BPL bit is disabled and the BPL, BP0, and BP1 and BP2 bits in the STATUS register can all be changed. As long as BPL bit is set to '0' or WP# pin is driven high (VIH) prior to the low-to-high transition of the CE# pin at the end of the WRSR instruction, the bits in the STATUS register can all be altered by the WRSR instruction. In this case, a single WRSR instruction can set the BPL bit to '1' to lock down the STATUS register as well as altering the BP0, BP1, and BP2 bits at the same time. See Table 4-1 for a summary description of WP# and BPL functions.

5.15 JEDEC Read ID

The JEDEC Read ID instruction identifies the device as SST25VF040B and the manufacturer as Microchip. The device information can be read from executing the 8-bit command, 9FH. Following the JEDEC Read ID instruction, the 8-bit manufacturer's ID, BFH, is output from the device. After that, a 16-bit device ID is shifted out on the SO pin.

Byte 1, BFH, identifies the manufacturer as Microchip. Byte 2, 25H, identifies the memory type as SPI Serial Flash. Byte 3, 8DH, identifies the device as SST25VF040B. The instruction sequence is shown in Figure 5-16. The JEDEC Read ID instruction is terminated by a low-to-high transition on CE# at any time during data output.

FIGURE 5-16: JEDEC READ ID SEQUENCE

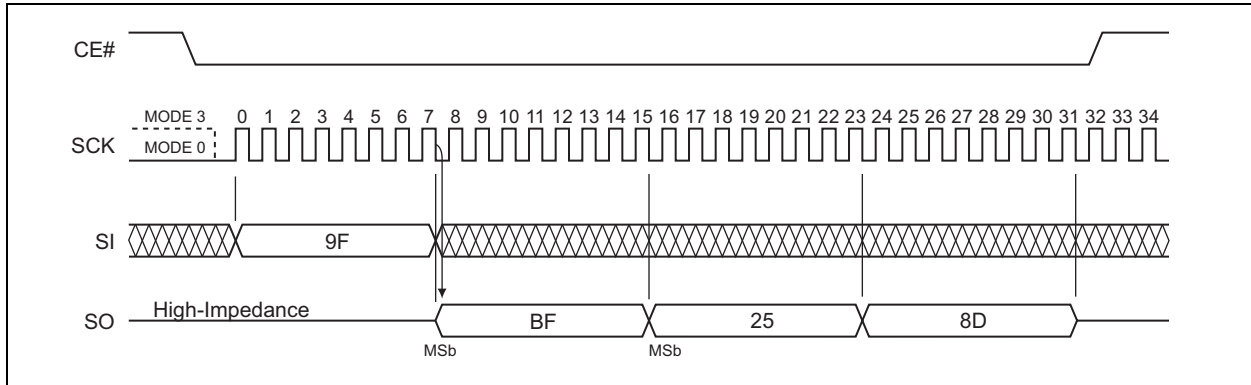


TABLE 5-2: JEDEC READ ID DATA

Manufacturer's ID	Device ID	
	Memory Type	Memory Capacity
Byte1	Byte 2	Byte 3
BFH	25H	8DH

5.16 Read ID (RDID)

The Read ID (RDID) instruction identifies the devices as SST25VF040B and manufacturer as Microchip. This command is backward compatible and should be used as default device identification when multiple versions of SPI Serial Flash devices are used in a design. The device information can be read from executing an 8-bit command, 90H or ABH, followed by address bits [A23-A0]. Following the Read ID instruction, the manufacturer's ID is located in address 00000H and the device ID is located in address 00001H. Once the device is in Read ID mode, the manufacturer's and device ID output data toggles between address 00000H and 00001H until terminated by a low-to-high transition on CE#.

Refer to Table 5-2 and Table 5-3 for device identification data.

FIGURE 5-17: READ ID SEQUENCE

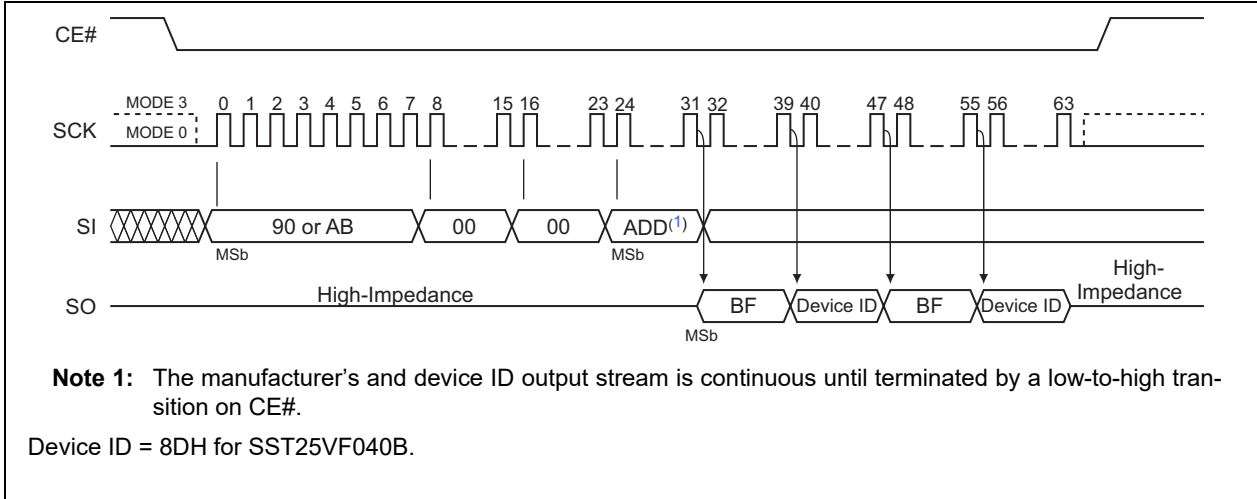


TABLE 5-3: PRODUCT IDENTIFICATION

	Address	Data
Manufacturer's ID	00000H	BFH
Device ID		
SST25VF040B	00001H	8DH

6.0 ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (†)

Temperature under bias	-55°C to +125°C
Storage temperature	-65°C to +150°C
DC voltage on any pin to ground potential	-0.5V to VDD+0.5V
Transient voltage (<20 ns) on any pin to ground potential	-2.0V to VDD+2.0V
Package power dissipation capability (TA = 25°C).....	1.0W
Surface mount solder reflow temperature	260°C for 10 seconds
Output short circuit current ⁽¹⁾	50 mA

† **NOTICE:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Note 1: Output shorted for no more than one second. No more than one output shorted at a time.

TABLE 6-1: OPERATING RANGE

Range	Ambient Temp.	VDD
Commercial	0°C to +70°C	2.7V-3.6V
Industrial	-40°C to +85°C	

TABLE 6-2: AC CONDITIONS OF TEST⁽¹⁾

Input Rise/Fall Time	Output Load
5 ns	CL = 30 pF

Note 1: See [Figure 6-2](#) and [Figure 6-3](#).

6.1 Power-Up Specifications

All functionalities and DC specifications are specified for a VDD ramp rate of greater than 1V per 100 ms (0V to 3.0V in less than 300 ms). See [Table 6-3](#) and [Figure 6-1](#) for more information.

TABLE 6-3: RECOMMENDED SYSTEM POWER-UP/POWER-DOWN TIMINGS

Symbol	Parameter	Min	Units
TPU-READ ⁽¹⁾	VDD Minimum to Read Operation	100	µs
TPU-WRITE ⁽¹⁾	VDD Minimum to Write Operation	100	µs

Note 1: This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

FIGURE 6-1: POWER-UP TIMING DIAGRAM

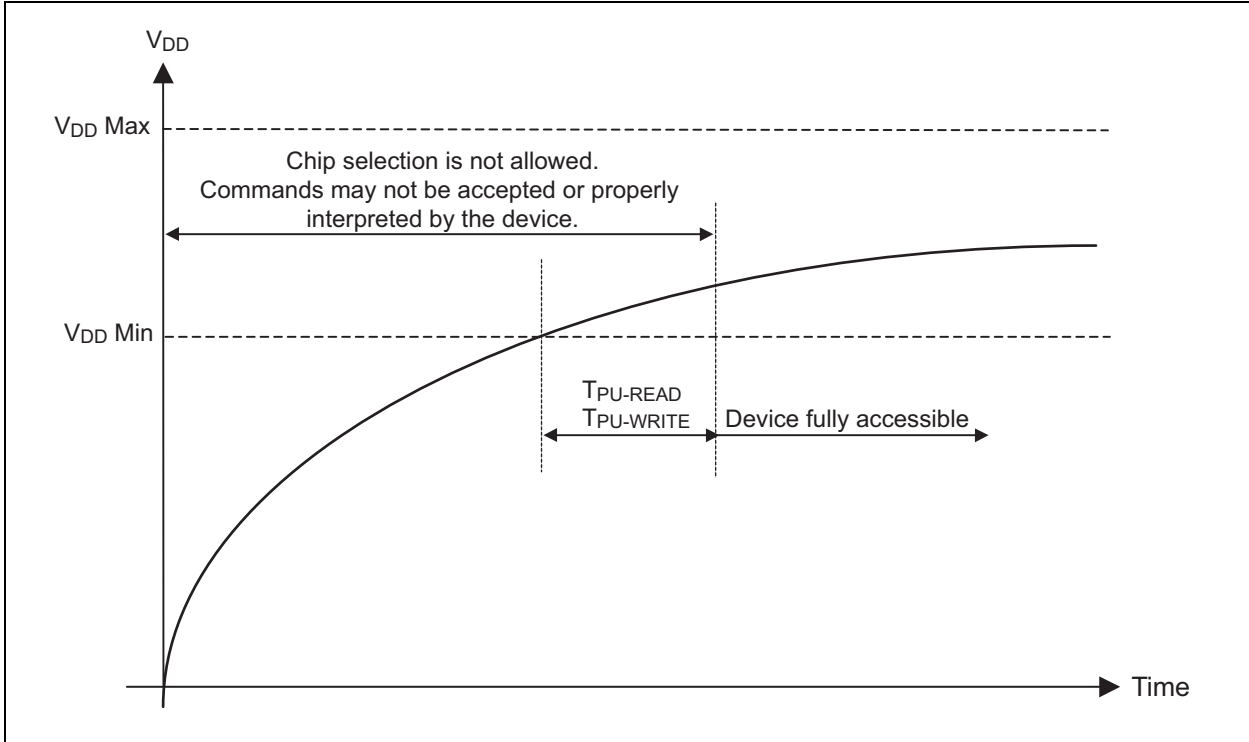


FIGURE 6-2: C INPUT/OUTPUT REFERENCE WAVEFORMS

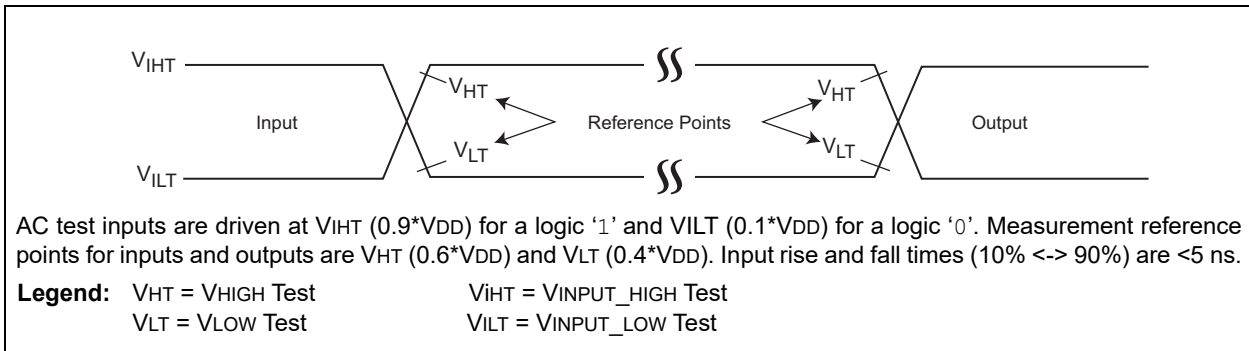
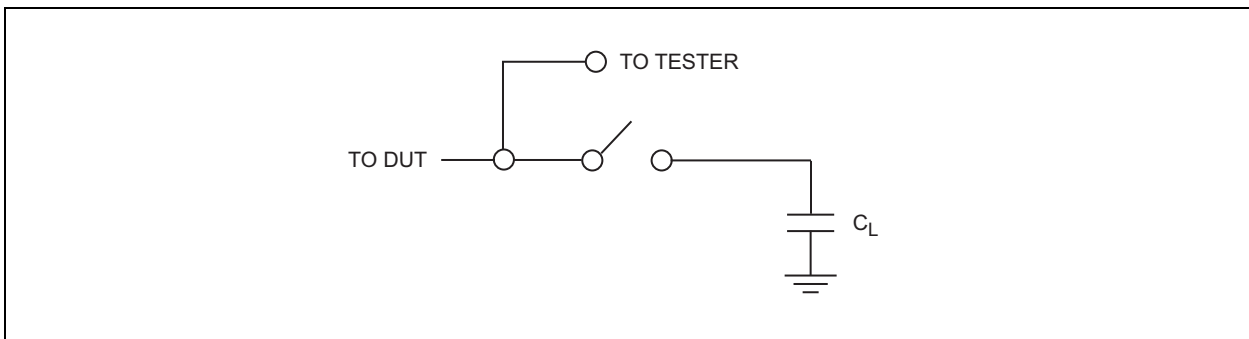


FIGURE 6-3: A TEST LOAD EXAMPLE



7.0 DC CHARACTERISTICS

TABLE 7-1: DC OPERATING CHARACTERISTICS

Symbol	Parameter	Limits			Test Conditions
		Min.	Max.	Unit	
IDDR1	Read Current	—	10	mA	CE# = 0.1 V _{DD} /0.9 V _{DD} @25 MHz, SO = Open
IDDR2	Read Current	—	15	mA	CE# = 0.1 V _{DD} /0.9 V _{DD} @50 MHz, SO = Open
IDDW	Program and Erase Current	—	30	mA	CE# = V _{DD}
ISB	Standby Current	—	30	μA	CE# = V _{DD} , V _{IN} = V _{DD} or V _{SS}
ILI	Input Leakage Current	—	1	μA	V _{IN} = GND to V _{DD} , V _{DD} = V _{DD} Max
ILO	Output Leakage Current	—	1	μA	V _{OUT} = GND to V _{DD} , V _{DD} = V _{DD} Max
VIL	Input Low Voltage	—	0.8	V	V _{DD} = V _{DD} Min
VIH	Input High Voltage	0.7*V _{DD}	—	V	V _{DD} = V _{DD} Max
VOL1	Output Low Voltage	—	0.2	V	I _{OL} = 100 μA, V _{DD} = V _{DD} Min
VOL2	Output Low Voltage	—	0.4	V	I _{OL} = 1.6 mA, V _{DD} = V _{DD} Min
VOH	Output High Voltage	V _{DD} -0.2	—	V	I _{OH} = -100 μA, V _{DD} = V _{DD} Min

TABLE 7-2: Capacitance (TA = 25°C, f = 1 MHz, Other Pins Open)

Parameter	Description	Test Condition	Maximum
C _{OUT} ⁽¹⁾	Output Pin Capacitance	V _{OUT} = 0V	12 pF
C _{IN} ⁽¹⁾	Input Capacitance	V _{IN} = 0V	6 pF

Note 1: This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 7-3: RELIABILITY CHARACTERISTICS

Symbol	Parameter	Minimum Specification	Unit	Test Method
NEND ⁽¹⁾	Endurance	10,000	Cycles	JEDEC Standard A117
TDR ⁽¹⁾	Data Retention	100	Years	JEDEC Standard A103
ILTH ⁽¹⁾	Latch Up	100 + I _{DD}	mA	JEDEC Standard 78

Note 1: This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

8.0 AC CHARACTERISTICS

TABLE 8-1: AC OPERATING CHARACTERISTICS

Symbol	Parameter	25 MHz		50 MHz		Units
		Min.	Max.	Min.	Max.	
FCLK ⁽¹⁾	Serial Clock Frequency	—	25	—	50	MHz
T _{SCKH}	Serial Clock High Time	18	—	9	—	ns
T _{SCKL}	Serial Clock Low Time	18	—	9	—	ns
T _{SCKR} ⁽²⁾	Serial Clock Rise Time (slew rate)	0.1	—	0.1	—	V/ns
T _{SCKF}	Serial Clock Fall Time (slew rate)	0.1	—	0.1	—	V/ns
T _{CE#} ⁽³⁾	CE# Active Setup Time	10	—	5	—	ns
T _{CEH} ⁽³⁾	CE# Active Hold Time	10	—	5	—	ns
T _{CHS} ⁽³⁾	CE# Not Active Setup Time	10	—	5	—	ns
T _{CHH} ⁽³⁾	CE# Not Active Hold Time	10	—	5	—	ns
T _{CPH}	CE# High Time	100	—	50	—	ns
T _{CHZ}	CE# High-to-High Z Output	—	15	—	8	ns
T _{CLZ}	SCK Low-to-Low Z Output	0	—	0	—	ns
T _{DS}	Data In Setup Time	5	—	2	—	ns
T _{DH}	Data In Hold Time	5	—	5	—	ns
T _{HL#}	HOLD# Low Setup Time	10	—	5	—	ns
T _{HHS}	HOLD# High Setup Time	10	—	5	—	ns
T _{HLH}	HOLD# Low Hold Time	10	—	5	—	ns
T _{HHH}	HOLD# High Hold Time	10	—	5	—	ns
T _{HZ}	HOLD# Low-to-High Z Output	—	20	—	8	ns
T _{LZ}	HOLD# High-to-Low Z Output	—	15	—	8	ns
T _{OH}	Output Hold from SCK Change	0	—	0	—	ns
T _V	Output Valid from SCK	—	15	—	8	ns
T _{SE}	Sector Erase	—	25	—	25	ms
T _{BE}	Block Erase	—	25	—	25	ms
T _{SCE}	Chip Erase	—	50	—	50	ms
T _{BP}	Byte Program	—	10	—	10	µs

Note 1: Maximum clock frequency for Read Instruction, 03H, is 25 MHz.

2: Maximum Rise and Fall time may be limited by T_{SCKH} and T_{SCKL} requirements.

3: Relative to SCK.

FIGURE 8-1: SERIAL INPUT TIMING DIAGRAM

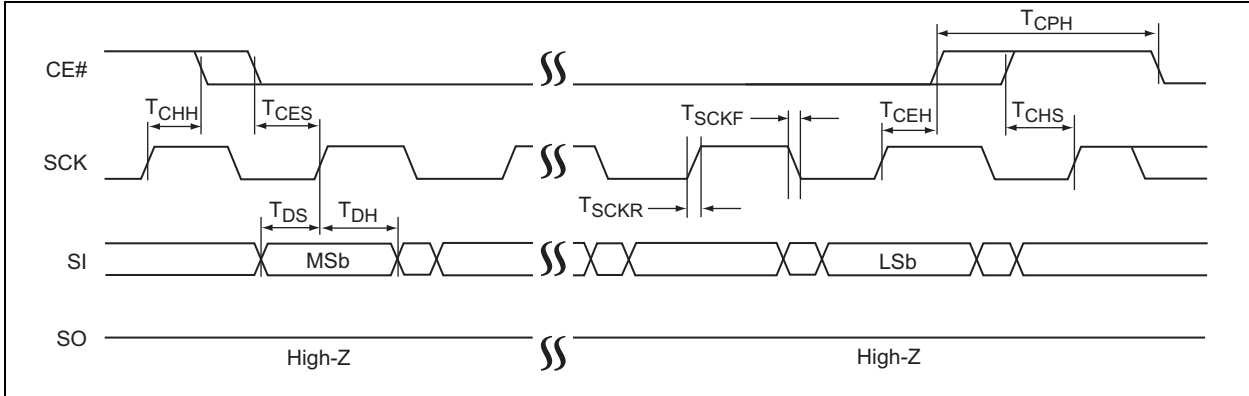


FIGURE 8-2: SERIAL OUTPUT TIMING DIAGRAM

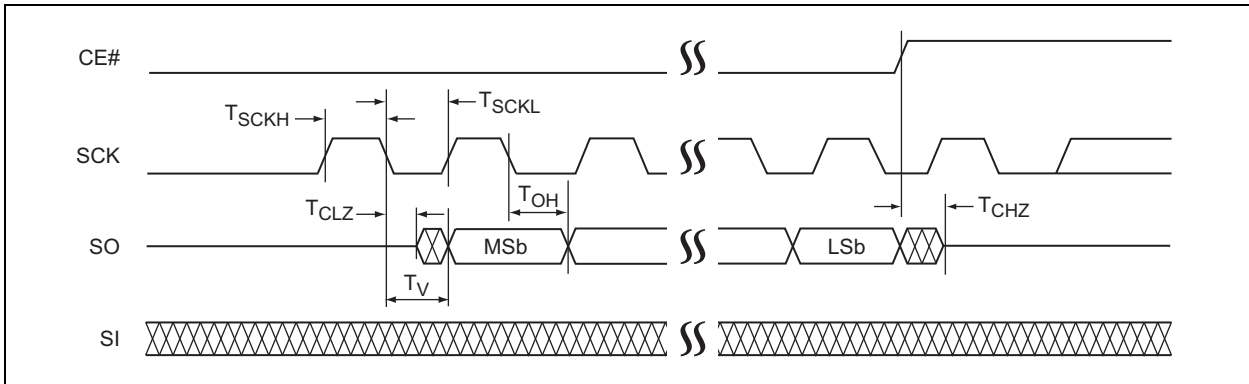
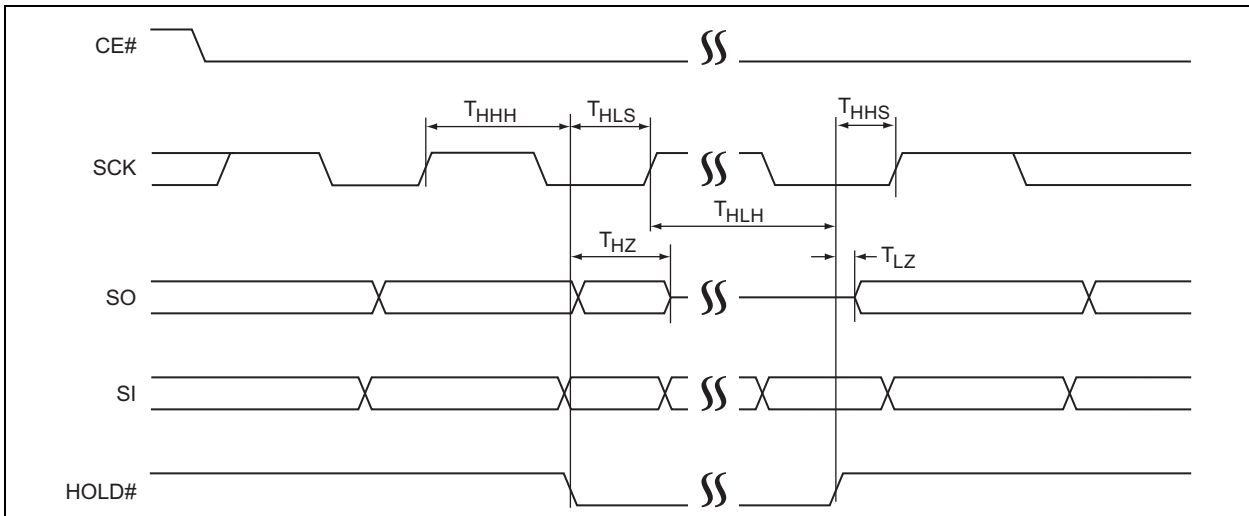


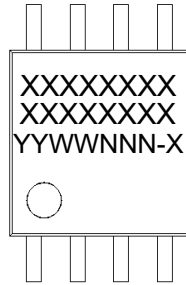
FIGURE 8-3: HOLD TIMING DIAGRAM



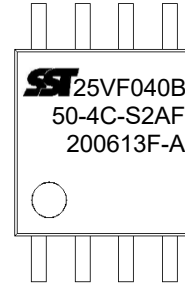
9.0 PACKAGING INFORMATION

9.1 Package Marking

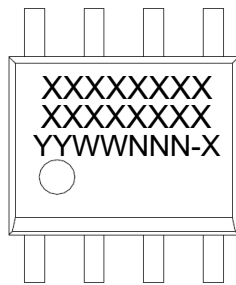
8-Lead SOIC (200 mils)



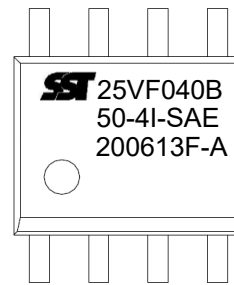
Example



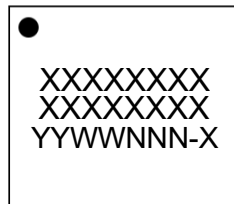
8-Lead SOIC (150 mils)



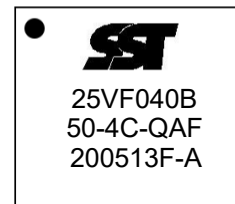
Example



8-Contact WSON (6 mm x 5 mm)



Example



Part Number	1 st Line Marking Codes	
	SOIC	WSON
SST25VF040B	SST25VF040B	25VF040B

Legend:	XX...X	Part number or part number code
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code (2 characters for small packages)
	(e3)	Pb-free JEDEC [®] designator for Matte Tin (Sn)

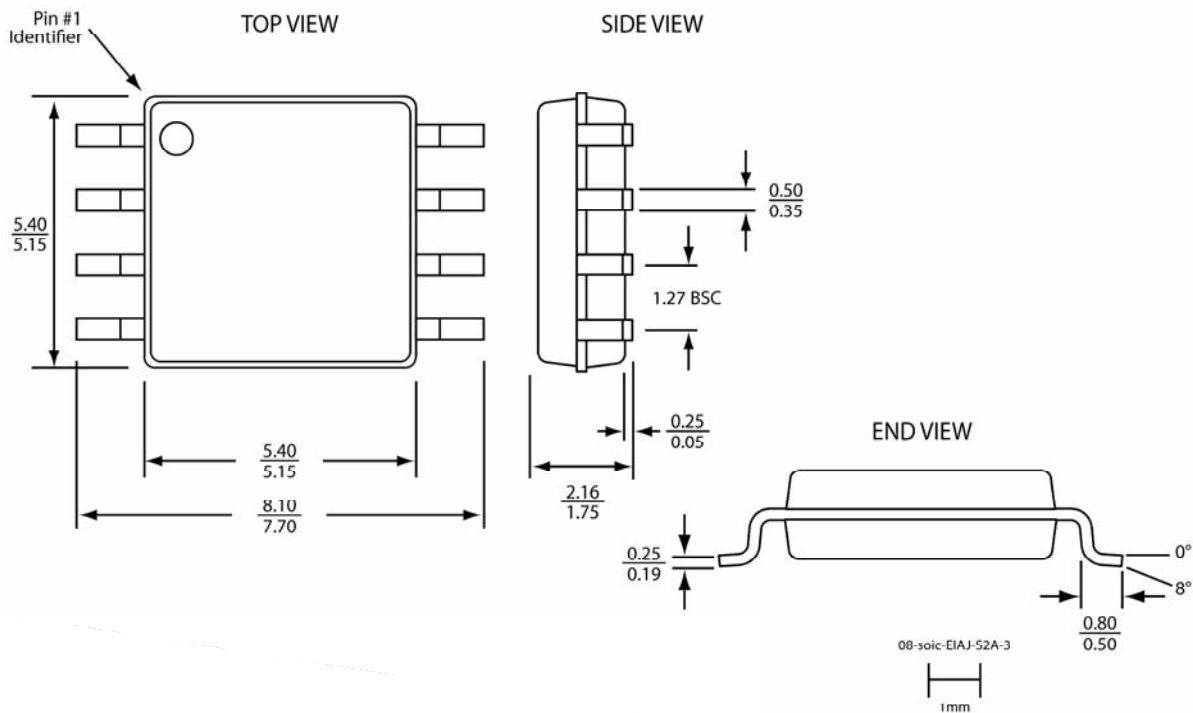
Note: For very small packages with no room for the Pb-free JEDEC[®] designator (e3), the marking will only appear on the outer carton or reel label.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

SST25VF040B

8-Lead Small Outline Integrated Circuit (S2AE/F) - .208 Inch Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



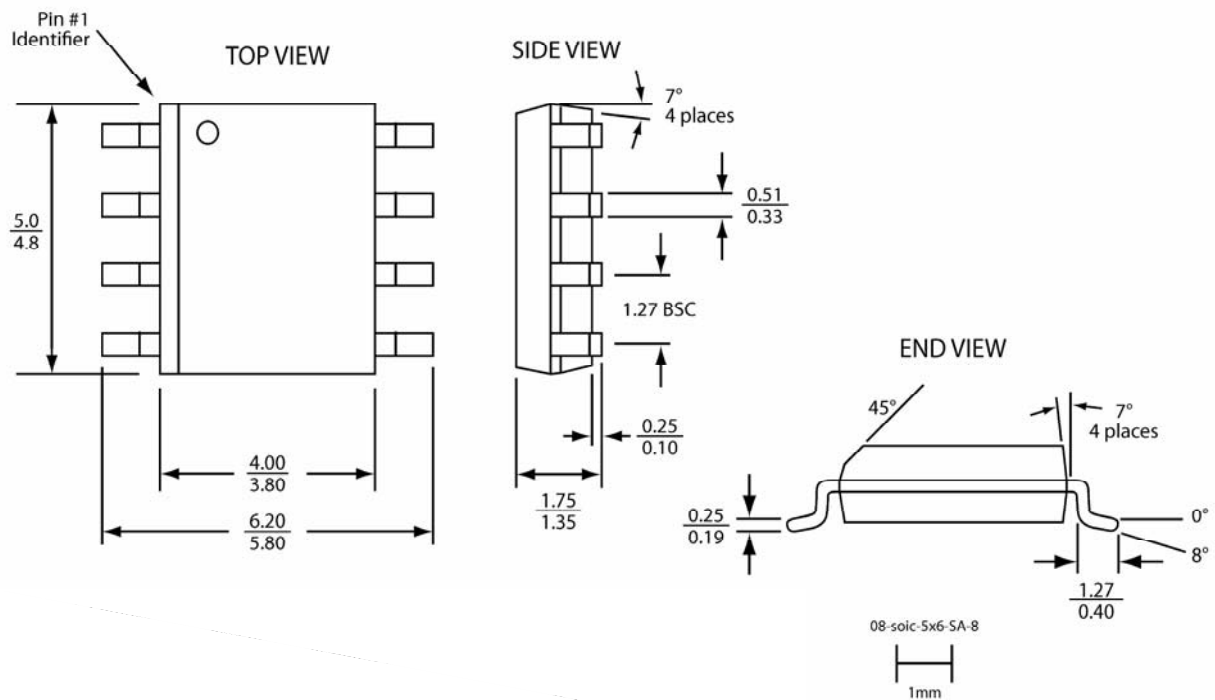
Note:

1. All linear dimensions are in millimeters (max/min).
2. Coplanarity: 0.1 mm
3. Maximum allowable mold flash is 0.15 mm at the package ends and 0.25 mm between leads.

SST25VF040B

8-Lead Small Outline Integrated Circuit (SAE/F) - 5x6 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



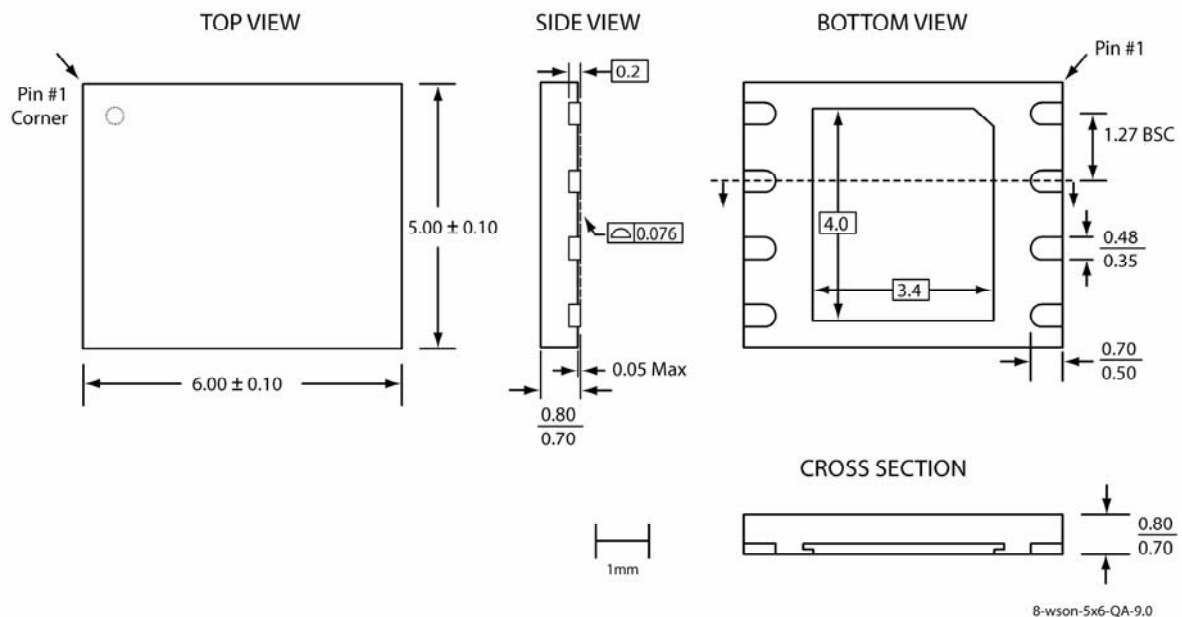
Note:

1. Complies with JEDEC publication 95 MS-012 AA dimensions, although some dimensions may be more stringent.
2. All linear dimensions are in millimeters (max/min).
3. Coplanarity: 0.1 mm
4. Maximum allowable mold flash is 0.15 mm at the package ends and 0.25 mm between leads.

SST25VF040B

8-Lead Very, Very Thin Small Outline No-Leads (QAE/F) - 5x6 mm Body [WSON]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Note:

1. All linear dimensions are in millimeters (max/min).
2. Untoleranced dimensions (shown with box surround) are nominal target dimensions.
3. The external paddle is electrically connected to the die back-side and possibly to certain VSS leads. This paddle can be soldered to the PC board; it is suggested to connect this paddle to the VSS of the unit. Connection of this paddle to any other voltage potential can result in shorts and/or electrical malfunction of the device.

APPENDIX A: REVISION HISTORY

Revision F (June 2020)

Corrected JEDEC ID.

Revision E (March 2020)

Updated standby current; Updated formatting to current template; Added package marking section; Updated Product Identification System Nickel plating note.

Revision D (July 2017)

Added Units column and corrected typo in Table 5-6.

Revision C (June 2015)

Corrected an address bit on page 13.

Revision B (February 2014)

EOL of all 80 MHz parts. Replacement parts are the 50 MHz counterparts found in this document. Removed all 80 MHz information. See DS20005264. Updated document to new format. Replaced all package drawings with drawings in the new format.

Revision A (September 2011)

Removed "Recommended System Power-up Timings" from page 29. Released document under letter revision system. Updated Spec number from S71295 to DS25051.

Revision 06 (February 2011)

Updated "Auto Address Increment (AAI) Word-Program", "End-of-Write Detection", and "Hardware End-of-Write Detection" on page 11. Revised Figures 4-8 and 4-9 on page 12. Updated document to new format.

Revision 05 (October 2009)

Added 50/33 MHz information throughout. Separated AC and DC Characteristics for SST25VF040B-50-4C-xxxF & SST25VF040B-80-4I-xxxE.

Revision 04 (June 2009)

Updated Product Ordering Information and Valid Combinations on page 29. Added "Power-Up Specifications" on page 22. Modified High-Speed-Read values in Table 4-4 on page 8 and "High-Speed-Read (50 MHz)" on page 9.

Revision 03 (March 2009)

Updated document to reflect upgraded clock frequency to 80 MHz globally. Updated Features. Changed maximum frequency to 80 MHz in Table 4-4 on page 8. Added IDDR3 to Table 5-3 on page 19. Added 80 MHz column to Table 5-6 on page 20. Updated Product Ordering Information and Valid Combinations on page 29.

Revision 02 (June 2007)

Added 8-Lead SOIC (150 mils) package drawing. Updated Features and Product Description to include new package information. Updated Pin-Assignment, Figure 2-1. Revised Figure 4-8 and Figure 4-9.

Revision 01 (January 2006)

Migrated document to a Data Sheet. Updated Surface Mount Solder Reflow Temperature information.

Revision 00 (September 2005)

Initial release of the document.

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- **General Technical Support** – Frequently Asked Questions (FAQ), technical support requests, online discussion groups, Microchip consultant program member listing
- **Business of Microchip** – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

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- Technical Support

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Technical support is available through the website at: <http://microchip.com/support>

SST25VF040B

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	-XX	-XX	-XXX	-[X] ⁽¹⁾			
Device	Operating Frequency	Minimum Endurance	Temp Range	Package	Package Modifier	Environmental Attribute	Tape and Reel Indicator
Device:	SST25VF040B	= 4 Mbit, 2.7V-3.6V, SPI Flash Memory					
Operating Frequency:	50	= 50 MHz					
Minimum Endurance:	4	= 10,000 cycles					
Temperature Range:	I C	= -40°C to +85°C (Industrial) = 0°C to +70°C (Commercial)					
Package:	S S2 Q	= SOIC (150 mil Body), 8-lead = SOIC (208 mil Body), 8-lead = WSON (6 mm x 5 mm Body), 8-contact					
Package Modifier:	A	= 8 leads or contacts					
Environmental Attribute:	E F	= Matte Tin finish = Nickel plating with Gold top (outer) layer finish or Matte Tin finish					
Tape and Reel Indicator:	Blank T	= Standard packaging (tube or tray) = Tape and Reel ⁽¹⁾					

Valid Combinations:

- a) SST25VF040B-50-4C-SAF
- b) SST25VF040B-50-4C-SAF-T
- c) SST25VF040B-50-4I-SAF
- d) SST25VF040B-50-4I-SAF-T
- e) SST25VF040B-50-4I-SAE
- f) SST25VF040B-50-4I-SAE-T
- g) SST25VF040B-50-4C-S2AF
- h) SST25VF040B-50-4C-S2AF-T
- i) SST25VF040B-50-4I-S2AF
- j) SST25VF040B-50-4I-S2AF-T
- k) SST25VF040B-50-4I-S2AE
- l) SST25VF040B-50-4I-S2AE-T
- m) SST25VF040B-50-4C-QAF
- n) SST25VF040B-50-4C-QAF-T
- o) SST25VF040B-50-4I-QAF
- p) SST25VF040B-50-4I-QAF-T
- q) SST25VF040B-50-4I-QAE
- r) SST25VF040B-50-4I-QAE-T

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